

**A CHARGE PUMP OR OTHER CHARGE STORAGE CAPACITOR
INCLUDING PZT LAYER FOR COMBINED USE
AS ENCAPSULATION LAYER AND DIELECTRIC LAYER
OF FERROELECTRIC CAPACITOR
AND A METHOD FOR MANUFACTURING THE SAME**

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a divisional filing of co-pending U.S. Patent Application Serial No. 10/288/137, filed November 4, 2002, which is a divisional filing of U.S. Patent Application Serial No. 09/863,365 filed May 22, 2001 (now U.S. Patent No. 6,493,673), which are hereby incorporated by reference in their entirety.

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a charge storage capacitor and more particularly, to a charge storage capacitor including an encapsulation layer that can also function as a dielectric layer of the charge storage capacitor.

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Discussion of the Related Art

Integrated circuit ferroelectric memory devices include an integrated circuit substrate which includes a cell region and a periphery region. A plurality of ferroelectric memory cells are formed in the cell region, including a plurality of ferroelectric capacitors. The ferroelectric capacitor in the ferroelectric memory cell includes a dielectric material that has a high dielectric constant and that can be polarized by an electric field, thus storing a memory data state. A polarization of the dielectric material remains until reversed by an opposite electrical field. This makes the dielectric memory cell non-volatile.

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Conventionally, capacitors with a single ferroelectric layer, such as a PZT-F layer (ferroelectric layer formed of PZT (lead zirconate titanate)), are used for making both switchable ferroelectric capacitors (data storage capacitors) and charge pump capacitors or other charge storage capacitors. However, it is very difficult to optimize the ferroelectric properties of a

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ferroelectric layer, such as a PZT-F layer, for high permittivity capacitor applications such as charge pumps or other charge storage capacitors. Further, conventionally, an encapsulation layer, such as a PZT-E layer (encapsulation layer formed of PZT (lead zirconate titanate)) is utilized only
5 for encapsulating and protecting the underlying ferroelectric capacitor including the PZT-F layer.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a charge storage capacitor that substantially obviates one or more of the problems due to
10 limitations and disadvantages of the related art.

An object of the present invention is to provide an improved charge storage capacitor.

Another object of the present invention is to provide a capacitor including a dielectric layer that is easy to optimize for both encapsulation and
15 high permittivity dielectric properties.

Another object of the present invention is to provide a capacitor having a high charge storage capability that has low leakage current and relatively linear capacitance dependence on voltage.

Another object of the present invention is to provide an integrated
20 circuit, including an improved charge storage and a ferroelectric memory cell, having a simple manufacture process.

Additional features and advantages of the invention will be set forth in the description, which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives
25 and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a
30 charge storage capacitor includes a bottom electrode, a dielectric layer

formed on the bottom electrode, and a local interconnect electrode formed on the dielectric layer.

In another aspect of the present invention, an integrated circuit including a capacitor includes a bottom, a first dielectric layer formed on the bottom electrode, a top electrode formed on the first dielectric layer, a second dielectric layer formed on the top electrode, wherein the second dielectric layer completely covers the top electrode, and a local interconnect electrode formed on the second dielectric layer.

In another aspect of the present invention, a charge storage capacitor includes a bottom electrode, a first dielectric layer formed on the bottom electrode, a second dielectric layer formed on the first dielectric layer, and a local interconnect electrode formed on the second dielectric layer.

In another aspect of the present invention, a method for forming a capacitor, includes the steps of forming a bottom electrode, forming an encapsulation layer on the bottom electrode, and forming a local interconnect electrode on the encapsulation layer.

In another aspect of the present invention, a method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, includes the steps of forming a bottom electrode of the charge storage capacitor and a bottom electrode of the data storage capacitor on an integrated circuit, forming a ferroelectric layer on the bottom electrode of the data storage capacitor, forming a top electrode on the ferroelectric layer, forming a first encapsulation layer on the bottom electrode of the charge storage capacitor and a second encapsulation layer on the bottom electrode of the data storage capacitor including the ferroelectric layer and the top electrode, wherein the first encapsulation layer and the second encapsulation are formed simultaneously, and forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer, wherein the first encapsulation layer is a dielectric layer of the charge storage capacitor.

In another aspect of the present invention, a method for forming an integrated circuit comprising a capacitor, includes the steps of forming a

bottom electrode, forming a ferroelectric layer on the bottom electrode, forming a top electrode on the ferroelectric layer, forming an encapsulation layer on the top electrode, wherein the encapsulation layer completely covers the top electrode, and forming a local interconnect electrode on the
5 encapsulation layer, wherein the ferroelectric layer includes PZT. °

In another aspect of the present invention, a method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, includes the steps of forming a bottom electrode of the charge storage capacitor and a bottom electrode of
10 the data storage capacitor on an integrated circuit substrate, forming a first ferroelectric layer on the bottom electrode of the charge storage capacitor and a second ferroelectric layer on the bottom electrode of the data storage capacitor, forming a first top electrode on the first ferroelectric layer and a second top electrode on the second ferroelectric layer, forming a first
15 encapsulation layer on the bottom electrode of the charge storage capacitor, including the first ferroelectric layer and the first top layer, forming a second encapsulation layer on the bottom electrode of the data storage capacitor, including the second ferroelectric layer and the second top layer, wherein the first encapsulation layer and the second encapsulation are formed
20 simultaneously, forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer, etching the first interlayer dielectric layer to form a first opening to expose the first encapsulation layer, etching the second interlayer dielectric layer and the second encapsulation layer to form a second opening
25 to expose the top electrode of the data storage capacitor, and forming a first local interconnect electrode in the first opening and a second local interconnect electrode in the second opening, simultaneously, wherein the first local interconnect electrode comprises part of the charge storage capacitor.

30 In another aspect of the present invention, a method for forming a capacitor, includes the steps of forming a bottom electrode, forming a ferroelectric layer on the bottom electrode, forming an encapsulation layer on

the ferroelectric layer, and forming a local interconnect electrode on the encapsulation layer.

In another aspect of the present invention, a method for forming an integrated circuit, comprising a charge storage capacitor and a ferroelectric memory cell including a data storage capacitor, includes the steps of forming
5 a bottom electrode of the charge storage capacitor and a bottom electrode of the data storage capacitor on an integrated circuit substrate, forming a first ferroelectric layer on the bottom electrode of the charge storage capacitor and a second ferroelectric layer on the bottom electrode of the data storage
10 capacitor, forming a top electrode layer on the first and second ferroelectric layers, etching the top electrode layer to remove from the first ferroelectric layer and to form a top electrode of the data storage capacitor on the second ferroelectric layer, forming a first encapsulation layer on the bottom electrode of the charge storage capacitor including the first encapsulation layer and a
15 second encapsulation layer on the bottom electrode of the data storage capacitor including the second ferroelectric layer and the top electrode, and forming a first interlayer dielectric layer on the first encapsulation layer and a second interlayer dielectric layer on the second encapsulation layer, wherein the first encapsulation layer and the second encapsulation are formed
20 simultaneously.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

25 The accompanying drawings, which are included to provide further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a cross sectional view of a ferroelectric memory cell;

FIGs. 2A-2F are sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a first embodiment of the present invention;

FIGs. 3A-3F are sequential cross sectional views of an integrated
5 circuit including a charge storage capacitor according to a second embodiment of the present invention;

FIGs. 4A-4F are sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a third embodiment of the present invention; and

10 FIGs. 5A-5F are sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of
15 the present invention, examples of which are illustrated in the accompanying drawings.

FIG. 1 shows a cross sectional view of a typical ferroelectric memory cell structure including a ferroelectric capacitor, which stores a memory data state. The ferroelectric capacitor includes a bottom electrode (BE) 111, a
20 PZT-F layer 112, and a top electrode (TE) 113. The ferroelectric memory cell further includes an encapsulation PZT (PZT-E) layer 114 formed on the ferroelectric capacitor to protect the underlying capacitor from being damaged during etching of the bottom electrode 111. Once the etching of the bottom electrode is finished, an interlevel dielectric (ILD) layer 150 is deposited.
25 Thereafter, the interlevel dielectric layer 150 and the PZT-E layer 114 are etched to form an opening so that a local interconnect electrode (LI) 115 can be formed to be in contact with the top electrode 113 through the opening.

FIGs. 2A-2E show sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a first embodiment of
30 the present invention. The integrated circuit includes the charge storage capacitor of the present invention and a ferroelectric memory cell including a

ferroelectric capacitor (data storage capacitor). The charge storage capacitor of the present invention and the data storage capacitor are formed simultaneously on an integrated circuit substrate by using the same process sequence.

5 FIG. 2A shows the integrated circuit including a section 210a, where the charge storage capacitor of the present invention is to be formed, and a section 210b, where the ferroelectric capacitor (data storage capacitor) is to be formed. The integrated circuit shown in FIG. 2A includes a CMOS underlayer coated with SiO₂ or other interlayer dielectric layer 241, with an
10 adhesion layer (not shown) formed thereon, and a bottom electrode layer 211 deposited thereon. The adhesion layer can be formed of Ti or TiO_x having a thickness of about 20 nm, for example. The bottom electrode layer can be made of Pt (Platinum) having a thickness of about 100 nm, for example. On the bottom electrode layer 211, a PZT-F 212 is deposited to a thickness in a
15 range of between 150-200 nm. Then, a top electrode layer 213 is deposited to a thickness of 150 nm, for example.

 Thereafter, the top electrode layer 213 in 210b is patterned by photolithography and reactive ion etching to form a top electrode (TE) 213b of the data storage capacitor. The top electrode layer 213 in 210a is completely
20 removed by the reactive ion etching (RIE), as shown in FIG. 2B.

 Thereafter, the PZT-F layer 212 in 210b is patterned by photolithography and reactive ion etching to form a PZT-F layer 212b. Simultaneously, the PZT-F 212 in 210a is completely removed by reactive ion etching, thus leaving a clean bottom electrode layer surface in 210a, as
25 shown in FIG. 2C.

 Then, an encapsulation layer formed of PZT (PZT-E layer) 214 is formed to a thickness in a range of between 30 to 200 nm, for example. Thereafter, the PZT-E layer 214 is patterned by photolithography and reactive ion etching to form a dielectric layer 214a of the charge storage capacitor and
30 an encapsulation layer 214b of the data storage capacitor. Also, the bottom electrode layer 211 is patterned by photolithography and reactive ion etching

to form a bottom electrode 211a of the charge storage capacitor and a bottom electrode 211b of the data storage capacitor, as shown in FIG. 2D.

Once the bottom electrodes 211a and 211b and the PZT-E layers 214a and 214b are formed, an interlayer dielectric layer 250 is deposited.

- 5 Thereafter, the interlayer dielectric layer 250 and the PZT-E layer 214b formed on the data storage capacitor in 210b are etched through to form an opening to provide access to the top electrode 213b of the data storage capacitor. Simultaneously, the interlayer dielectric layer 250 formed in 210a is etched, without etching the PZT-E layer 214a, to form an opening therein, as
10 shown in FIG. 2E.

- Thereafter, a local interconnect layer 215 is deposited and patterned by photolithography and reactive ion etching to form a local interconnect electrode 215b of the ferroelectric memory cell in 210b and a local interconnect electrode 215a of the charge storage capacitor in 210a,
15 simultaneously, as shown in FIG. 2F. The local interconnect electrode 215a is also a second electrode of the charge storage capacitor. The local interconnect layer can be made of conductive materials, such as TiN and Al, for example.

- In this embodiment, the charge storage capacitor includes the
20 encapsulation PZT (PZT-E) layer 214a as a dielectric layer of the capacitor. Further, in this embodiment, the bottom electrode (BE) 211a is used as a first electrode and the local interconnect layer (LI) 215a is used as a second electrode of the charge storage capacitor.

- The PZT-E layer 214 can be formed by electron beam deposition, flash
25 deposition, ion plating, Rf-magnetron sputtering, ion beam sputtering, laser ablation, molecular beam epitaxy (MBE), chemical vapor deposition (CVD), plasma CVD or MOCVD, or sol-gel method. By depositing the PZT layer with properly adjusted Pb concentration with high temperature deposition, up to 700 °C, or by changing deposited Pb concentration, enhanced linear dielectric
30 response and reduced leakage current can be provided. Further, as part of the manufacture process, it is also possible to plasma damage the PZT layer

during the etching of the bottom electrode layer and the PZT-E layer, thereby improving the linear dielectric performance of the PZT layer.

FIGs. 3A-3G show sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a second
5 embodiment of the present invention. The charge storage capacitor and a ferroelectric capacitor (data storage capacitor) are formed simultaneously on an integrated circuit substrate by using the same process sequence.

FIG. 3A shows the integrated circuit including a section 310a, where the charge storage capacitor is to be formed, and a section 310b, where the data storage capacitor is to be formed. The integrated circuit shown in FIG.
10 3A includes a CMOS underlayer coated with SiO₂ or other interlayer dielectric layer 341, with an adhesion layer (not shown) formed thereon, and a bottom electrode layer 311 deposited thereon. The adhesion layer can be formed of Ti or TiO_x having a thickness of about 20 nm, for example. The bottom
15 electrode layer can be made of Pt (Platinum) having a thickness of about 100 nm, for example. On the bottom electrode layer 311, a PZT-F 312 is deposited to a thickness in a range of between 150-200 nm. Then, a top electrode layer 313 is deposited to a thickness of 150 nm, for example.

Thereafter, the top electrode layer 313 is patterned by photolithography and reactive ion etching to form a top electrode (TE) 313a of the charge
20 storage capacitor and a top electrode (TE) 313b of the data storage capacitor, as shown in FIG. 3B.

Thereafter, the PZT-F 312 layer in 310b is patterned by photolithography and reactive ion etching to form a PZT-F layer 312b.
25 Simultaneously, the PZT-F 312 in 310a is patterned by photolithography and reactive ion etching to form a PZT-F layer 312a, as shown in FIG. 3C. An area of the PZT-F layer 312a must be larger than an area of the charge storage capacitor.

Then, a PZT-E layer 314 is formed to a thickness in a range of
30 between 30 to 200 nm, for example. Thereafter, the PZT-E layer 314 is patterned by photolithography and reactive ion etching to form a dielectric layer 314a of the charge storage capacitor and an encapsulation layer 314b of

the data storage capacitor. Also, the bottom electrode layer 311 is patterned by photolithography and reactive ion etching to form a bottom electrode 311a of the charge storage capacitor and a bottom electrode 311b of the data storage capacitor, as shown in FIG. 3D. An area of the PZT-E layer 314a and the bottom electrode (BE) 311a of the charge storage capacitor must be longer than an area of the shorter of the two electrodes constituting the charge storage capacitor.

Once the bottom electrodes 311a and 311b and the PZT-E layers 314a and 314b are formed, an interlayer dielectric layer 350 is deposited. Thereafter, the interlayer dielectric layer 350 and the PZT-E layer 314b formed on the data storage capacitor in 310b are etched through to form an opening to provide access to the top electrode 313b of the data storage capacitor. Simultaneously, the interlayer dielectric layer 350 formed in 310a is etched, without etching the PZT-E layer 314a, to form an opening therein, as shown in FIG. 3E.

Thereafter, a local interconnect layer 315 is deposited and patterned by photolithography and reactive ion etching to form a local interconnect electrode (LI) 315b of the ferroelectric memory cell in 310b and a local interconnect electrode 315a of the charge storage capacitor in 310a, as shown in FIG. 3F. The local interconnect electrode 315a of the charge storage capacitor is also a second electrode of the charge storage capacitor. The local interconnect layer can be made of conductive materials, such as TiN and Al, for example.

In this embodiment, the charge storage capacitor includes the top electrode 313a, the PZT-E layer 314a, and the local interconnect electrode 315a formed on the bottom electrode 311a and the PZT-F layer 312a. In this embodiment, the bottom electrode 311a and the PZT-F layer 312a remain as part of the capacitor structure, but they are electrically isolated from the rest of the charge storage capacitor. There is an electrical connection to the top electrode 313a, but there is no electrical connection to the bottom electrode 311a, thus neither the bottom electrode 311a nor the PZT-F layer 312a has any electrical function in the charge storage capacitor.

FIGs. 4A-4G show sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a third embodiment of the present invention. The charge storage capacitor and a ferroelectric capacitor (data storage capacitor) are formed simultaneously on an
5 integrated circuit substrate by using the same process sequence.

FIG. 4A shows the integrated circuit including a section 410a, where the charge storage capacitor is to be formed, and a section 410b, where the data storage capacitor is to be formed. The integrated circuit shown in FIG. 4A includes a CMOS underlayer coated with SiO₂ or other interlayer dielectric
10 layer 441, with an adhesion layer (not shown) formed thereon, and a bottom electrode layer 411 deposited thereon. The adhesion layer can be formed of Ti or TiO_x having a thickness of about 20 nm, for example. The bottom electrode layer can be made of Pt (Platinum) having a thickness of about 100 nm, for example. On the bottom electrode layer 411, a PZT-F 412 is
15 deposited to a thickness in a range of between 150-200 nm. Then, a top electrode layer 413 is deposited to a thickness of 150 nm, for example.

Thereafter, the top electrode layer 413 in 410b is patterned by photolithography and reactive ion etching to form a top electrode 413b of the data storage capacitor and the top electrode layer 413 in 410a is removed by
20 reactive ion etching, as shown in FIG. 4B.

Thereafter, the PZT-F 412 in 410b is patterned by photolithography and reactive ion etching to form PZT-F layers 412a and 412b, as shown in FIG. 4C.

Then, a PZT-E layer 414 is formed to a thickness in a range of
25 between 30 to 200 nm, for example. Thereafter, the PZT-E layer 414 is patterned by photolithography and reactive ion etching to form 414a and 414b. Also, the bottom electrode layer 411 is patterned by photolithography and reactive ion etching to form a bottom electrode 411a of the charge storage capacitor and a bottom electrode 411b of the data storage capacitor,
30 as shown in FIG. 4D.

Once the bottom electrodes 411a and 411b and the PZT-E layers 414a and 414b are formed, an interlayer dielectric layer 450 is deposited.

Thereafter, the interlayer dielectric layer 450 and the PZT-E layer 414b formed on the data storage capacitor in 410b are etched through to form an opening to provide access to the top electrode 413b of the data storage capacitor. Simultaneously, the interlayer dielectric layer 450 formed in 410a is etched, without etching the PZT-E layer 414a, to form an opening therein, as shown in FIG. 4F.

Thereafter, a local interconnect layer 415 is deposited and patterned by photolithography and reactive ion etching to form a local interconnect electrode 415b of the ferroelectric memory cell in 410b and a local interconnect electrode 415a of the charge storage capacitor in 410a, as shown in FIG. 4G. The local interconnect electrode 415a is also a second electrode of the charge storage capacitor. The local interconnect layer can be made of conductive materials, such as TiN and Al, for example.

In this embodiment, the charge storage capacitor includes both the PZT-F layer and the PZT-E layer as a dielectric layer of the capacitor. Since the PZT-E layer can be easily optimized for better charge storage characteristics, such as voltage linearity, for example, than the PZT-F layer, the combined PZT-F and PZT-E layers will improve the capacitor performance of the charge storage capacitor in comparison with using the PZT-F layer alone.

In a method for forming the PZT-E layer and the PZT-F layer, in addition to using different processes, different compositions, which include changing the concentrations of Pb, Zr, and/or Ti, as well as dopant concentrations, can be used. For example, the PZT-E layer can be deposited with a lower Pb concentration than that of the PZT-F layer, thereby providing the layer with reduced leakage current without a dramatic decrease in permittivity. As part of the processing, it is also possible to plasma damage the PZT-E layer during the top electrode, bottom electrode, PZT-E, and PZT-F etching processes, thereby improving the linear dielectric performance of the PZT-E layer.

FIGs. 5A-5G show sequential cross sectional views of an integrated circuit including a charge storage capacitor according to a fourth embodiment

of the present invention. The charge storage capacitor and a ferroelectric capacitor (data storage capacitor) are formed simultaneously on an integrated circuit substrate by using the same process sequence.

FIG. 5A shows the integrated circuit including a section 510a, where
5 the charge storage capacitor is to be formed, and a section 510b, where the data storage capacitor is to be formed. The integrated circuit shown in FIG. 5A includes a CMOS underlayer coated with SiO₂ or other interlayer dielectric layer 541, with an adhesion layer (not shown) formed thereon, and a bottom electrode layer 511 deposited thereon. The adhesion layer can be formed of
10 Ti or TiO_x having a thickness of about 20 nm, for example. The bottom electrode layer can be made of Pt (Platinum) having a thickness of about 100 nm, for example. On the bottom electrode layer 511, a PZT-F 512 is deposited to a thickness in a range of between 150-200 nm. Then, a top electrode layer 513 is deposited to a thickness of 150 nm, for example.

15 Thereafter, the top electrode layer 513 is patterned by photolithography and reactive ion etching to form a top electrode 513b of the data storage capacitor and a top electrode 513a of the charge storage capacitor, as shown in FIG. 5B.

Thereafter, the PZT-F 512 in 510b is patterned by photolithography
20 and reactive ion etching to form a PZT-F layer 513b. Simultaneously, the PZT-F 513 in 510a is patterned by photolithography and reactive ion etching to form a PZT-F layer 513a, as shown in FIG. 5C.

Then, a PZT-E layer 514 is formed to a thickness in a range of
between 30 to 200 nm, for example. Thereafter, the PZT-E layer 514 is
25 patterned by photolithography and reactive ion etching to form an encapsulation layer 514b of the data storage capacitor and a dielectric layer 514a of the charge storage capacitor. Also, the bottom electrode layer 511 is patterned by photolithography and reactive ion etching to form a bottom electrode 511a of the charge storage capacitor and a bottom electrode 511b
30 of the data storage capacitor, as shown in FIG. 5D.

Once the bottom electrodes 511a and 511b and the PZT-E layers 514a and 514b are formed, an interlayer dielectric layer 550 is deposited.

Thereafter, the interlayer dielectric layer 550 and the PZT-E layer 514b formed on the data storage capacitor in 510b are etched through to form an opening to provide access to the top electrode 513b of the data storage capacitor. Simultaneously, the interlayer dielectric layer 550 formed on the charge storage capacitor in 510a is etched, without etching the PZT-E layer 514a, to form an opening therein, as shown in FIG. 5F.

Thereafter, a local interconnect layer 515 is deposited and patterned by photolithography and reactive ion etching to form a local interconnect electrode 515b of the ferroelectric memory cell in 510b and a local interconnect electrode 515a of the charge storage capacitor in 510a, as shown in FIG. 5G. The local interconnect electrode 515a is a second electrode of the charge storage capacitor. The local interconnect layer can be made of conductive materials, such as TiN and Al, for example.

The charge storage capacitor in this embodiment has a similar structure to the structure of the second embodiment of the present invention, except for the bottom electrode 511a being a first electrode of the charge storage capacitor in this embodiment. The charge storage capacitor in this embodiment includes both the PZT-F layer 512a and the PZT-E layer 514a, with the bottom electrode 511a being the first electrode and the local interconnect electrode 515a being the second electrode of the charge storage capacitor. In this embodiment, there is no electrical connection to the top electrode 513a. The top electrode 513a is effectively a floating electrode. Effectively, there are two capacitors connected in series. The entire stack, including the bottom electrode 511a, the PZT-F layer 512a, the top electrode 513a, the PZT-E layer 514a, and the local interconnect electrode 515a, is electrically active. The charge storage capacitor of this embodiment provides improved linearity and higher breakdown voltage in comparison with a capacitor formed with only a PZT-F layer.

In the present invention, the PZT-E layer can be replaced with other materials, such as other Pb-based perovskite dielectrics, aluminum oxide, tantalum oxide, BaTiO₃, or other dielectrics, for example.

The charge storage capacitor of the present invention can be used as part of the ferroelectric memory cell or as part of the circuitry in the periphery outside the ferroelectric memory cell.

5 By using the structures and the methods described above, a memory cell with an encapsulation layer and a charge storage capacitor using the encapsulation layer as a dielectric can be formed simultaneously, thus providing a simplified manufacturing process. Further, by using the structures and the methods described above, charge pumps or other charge storage capacitors having a high permittivity dielectric can be formed.

10 It will be apparent to those skilled in the art that various modifications and variations can be made in the charge storage capacitor of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention if they come within the scope of any claims and their
15 equivalents.